

forming a second memory cells as a commode to include a chalcogenide glass material having a changeable resistance and cathode and anode electrodes spaced apart and in contact with said chalcogenide glass material;

forming said anode electrodes of said memory cells as a common anode, wherein said common anode comprises a middle conductive layer and a layer of silver on opposite sides of said middle conductive layer.

24. (Twice Amended) A method as in claim 23 further comprising forming a column line conductor electrically coupled to a second active region of a first access transistor.

27. (Twice Amended) A method as in claim 26 wherein said first and second memory cells are formed to be coupled to different column lines by said first and second access transistors.

28. (Twice Amended) A method as in claim 17 wherein said first and second memory cells are formed to be connected to the same column line by said first and second access transistors.

Please add the following new claims:

47. A method of fabricating a memory device, comprising:

forming a first memory element comprising a first chalcogenide material layer and a first metal containing layer;

forming a second memory element comprising a second chalcogenide material and a second metal containing layer; said second memory element fabricated to being stacked over and arranged as a mirror image of said first memory element;

forming a first electrode in electrical communication with one side of said first memory element;

CH forming a second electrode in electrical communication with one side of said second memory element; and

forming a common electrode in electrical communication with a second side of each of said memory elements.

48. A method as in claim 47 wherein said metal containing layers of said first and second memory elements each contain silver.

49. A method as in claim 48 wherein said metal containing layers are silver layers.

50. A method as in claim 47 wherein said common electrode is an anode electrode having said metal containing layers of said first and second memory elements on opposite sides thereof.

51. A method as in claim 50 wherein said metal containing layers are silver layers.

52. A method as in claim 47 further comprising forming an access device for enabling access to at least one of said memory elements.

53. A method as in claim 52 further comprising forming a respective access device for each of said memory elements.

54. A method as in claim 47 further comprising forming an access circuitry for separately accessing said memory elements.

55. A multi-cell programmable microelectric device comprising:

a first electrode of a first type;

a second electrode of a second type;

a first ion conductive material of a first resistance interposed between the first electrode and the second electrode;

a third electrode of a first type; and

a second ion conductive material of a second resistance interposed between the second electrode and the third electrode.

56. The multi-cell programmable microelectric device of claim 55, wherein the first and third electrodes comprise an indifferent electrode material and the second electrode comprises an indifferent electrode material.

57. A method of forming a multi-cell programmable device, the method comprising the steps of:

forming a first electrode on a surface of a substrate;

forming a first ion conductor portion overlying the first electrode;

forming a second electrode overlying the first ion conductor portion;

forming a second ion conductor portion overlying the second electrode; and

forming a third electrode overlying the second ion conductor portion.